

Using a buck converter in an inverting buck-boost topology

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Introduction

Most practical electronic devices require an input voltage source. This may be a battery for handheld or portable devices, a 115-V AC line source or “wall wart” for home consumer electronics, or a regulated DC voltage bus for industrial or telecommunications applications. Typically, the input voltage source must be converted to one or more lower voltage sources to power individual circuits such as processors, memory, FPGAs, or other logic. Buck converters are commonly used to derive the required input voltage from a higher voltage source. In some cases, generating a negative voltage from a positive input voltage source may be required. These applications can include audio amplifiers, line drivers and receivers, or instrumentation amplifiers. In such instances it is possible to configure the buck converter into an inverting buck-boost topology, where the output voltage is negative with respect to ground.

Basic buck topology

To understand the inverting buck-boost circuit operation, first consider the basic topology of the buck converter as shown in Figure 1. The components inside the box with a

blue dotted outline are typically integrated into the converter’s integrated circuit, while those outside are required external components.

When the FET switch is on, the voltage across the inductor is $V_{IN} - V_{OUT}$, and the current through the inductor increases at a rate of

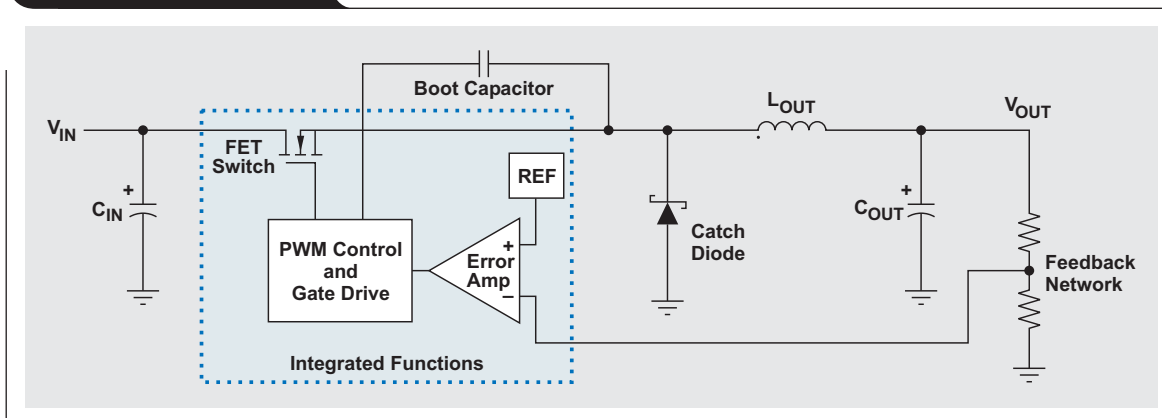
$$\frac{di}{dt} = \frac{V_{IN} - V_{OUT}}{L}$$

When the switch is off, the inductor voltage reverses to keep the inductor current continuous. Assuming that the voltage drop across the diode is small, the inductor current ramps down at a rate of $di/dt = V_{OUT}/L$. The steady-state load current is always carried by the inductor during both the on and off times of the FET switch. The average inductor current is equal to the load current, and the peak-to-peak inductor ripple current is

$$I_{L(PP)} = \frac{(V_{IN} - V_{OUT})D}{f_{SW}L},$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, D is the duty cycle V_{OUT}/V_{IN} , f_{SW} is the switching frequency, and L is the output inductance.

Figure 1. Buck topology



Inverting buck-boost topology

Compare the preceding operation to that of the inverting buck-boost topology shown in Figure 2. The inductor and catch diode have switched places relative to the buck converter of Figure 1; and the output capacitor is reversed in polarity, as the output voltage is negative. During operation, when the FET switch is on, the voltage across the inductor is V_{IN} and the current ramps up at a rate of $di/dt = V_{IN}/L$. While the FET switch is on, the entire load current is supplied by energy stored in the output capacitor. When the FET switch turns off, the inductor reverses polarity to keep the inductor current continuous. The voltage across the inductor is approximately V_{OUT} , and the inductor current decreases at a rate of $di/dt = -V_{OUT}/L$. During the off time, the inductor supplies current both to the load and to replenish the energy lost by the capacitor during the on time. So for the buck-boost circuit, the average inductor current is

$$I_L = \frac{I_{OUT}}{1-D},$$

and the peak-to-peak inductor current is

$$I_{L(PP)} = \frac{V_{IN}D}{f_{SW}L}.$$

The duty cycle, D , is approximately

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}}.$$

These basic differences in circuit operation are important when the buck converter is used as a buck-boost converter.

Design considerations

When a nonsynchronous buck converter is used in an inverting buck-boost configuration, certain considerations must be made. The design equations are presented in simplified form with the semiconductors idealized and other component losses neglected. To implement the buck-boost topology of Figure 2, the buck-converter ground pin is connected to V_{OUT} , and the positive lead of the output capacitor is connected to ground. The voltage across the device's V_{IN} pin to GND is then $V_{IN} - (-V_{OUT})$, rather than

just V_{IN} as in the buck converter. This combined voltage must be less than the specified V_{IN} of the chosen device.

The operating duty cycle is

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}},$$

and the average inductor current is

$$I_{L(avg)} = \frac{I_{OUT}}{1-D}.$$

These values also differ from those of the buck converter, whose duty cycle, $D = V_{OUT}/V_{IN}$, and average inductor current are equal to the output current.

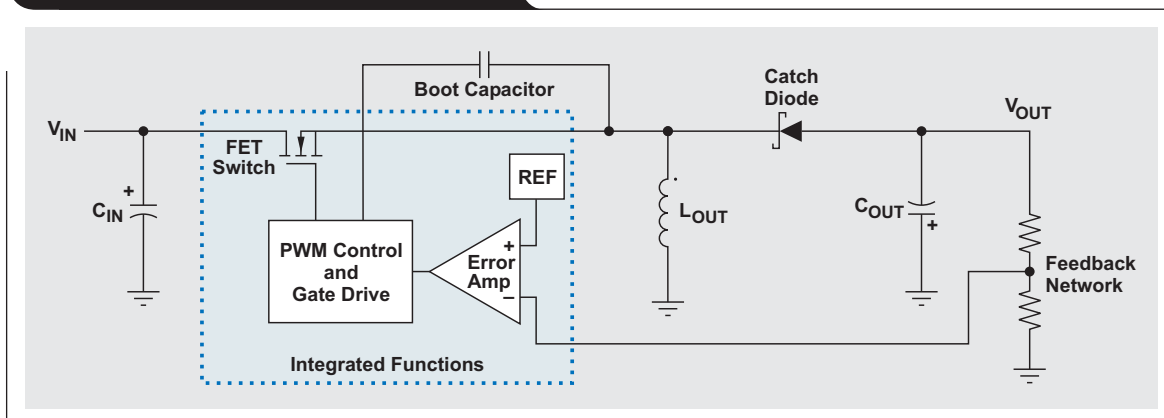
Since the average output current cannot exceed the device's rated output, the available load current is reduced by a factor of $1 - D$. So for this design, the maximum available DC load current is $I_{SW} \times (1 - D) = I_{Load}$, where I_{SW} is the average rated current of the high-side switch FET.

In addition, the inductor AC ripple current should be kept small for several reasons. The peak inductor current, which is the average inductor current plus half the peak-to-peak AC current, must be below the internal circuit's current limit. The inductor AC ripple current also determines the DC output current below which the circuit begins to operate in the discontinuous conduction mode. This operation mode occurs when the DC output current is equal to half the peak-to-peak AC current. In general, this restriction will be more severe than the current limit. The ripple current also contributes significantly to the output-voltage ripple. Lower inductor ripple currents provide cleaner output voltages.

For the inverting buck-boost converter, there are significant differences between discontinuous- and continuous-mode operation. Designs that are stable in the discontinuous mode may become unstable when increased load current causes them to operate in the continuous mode, during which the feedback loop contains a right-half-plane zero.¹

A bypass capacitor from V_{IN} to ground and from V_{IN} to V_{OUT} should be used on the input. The bypass from V_{IN} to V_{OUT} is across the device voltage input.

Figure 2. Inverting buck-boost topology



Typical waveforms

To demonstrate some of the performance differences between the two topologies, a test circuit was constructed for each type. Both circuits use a 24-V input. The buck converter has a 5-V output at 2 A, while the inverting buck-boost converter has a -5-V output, also at 2 A. Output voltage ripple and switching-node waveforms for the inverting buck-boost and buck converters are shown in Figures 3 and 4. Note that the switching-node voltage varies from V_{IN} to V_{OUT} for the inverting buck-boost converter, and from V_{IN} to ground for the buck converter. The ground reference line is indicated by the C2 marker at the left edge of each figure. Also observe that the output voltage ripple does not show the linear ramp characteristic typical of the buck converter. In the buck converter, the average inductor current is delivered to the load while the AC portion is shunted to ground through the output-filter capacitor. The primary component of the ripple voltage is the AC ripple current times the equivalent series resistance of the output cap, resulting in a waveform resembling a ramp that

rises during the FET switch on time and falls during the switch off time. For the inverting buck-boost converter, the output capacitor supplies the load current during the switch on time and is recharged during the switch off time. This charge-and-discharge cycle is superimposed with the AC ripple current to create a more complex ripple current as shown in the figures. Remember that the output voltage is negative, so the positive portions of the waveform represent the output becoming less negative, or the discharge portion of the cycle.

Figures 5 and 6 show the current flowing in the high-side switch for the inverting buck-boost and buck converters, respectively, each with the same load current of 2 A. The positive pulse represents the current flowing through the switch into the inductor during the conduction time. When the switch is off, the inductor current for the inverting buck-boost converter in Figure 5 must remain continuous and flows through the catch diode rather than the high-side switching element. For the buck converter in Figure 6, the average current during conduction is equal to the output

Figure 3. Inverting buck-boost output voltage ripple and switching-node voltage

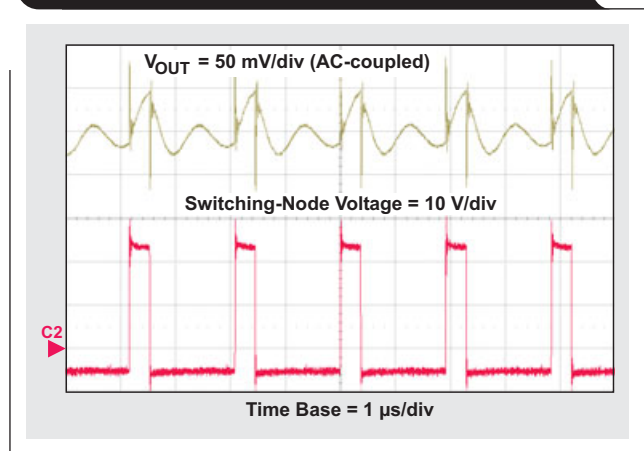


Figure 5. Inverting buck-boost switch current

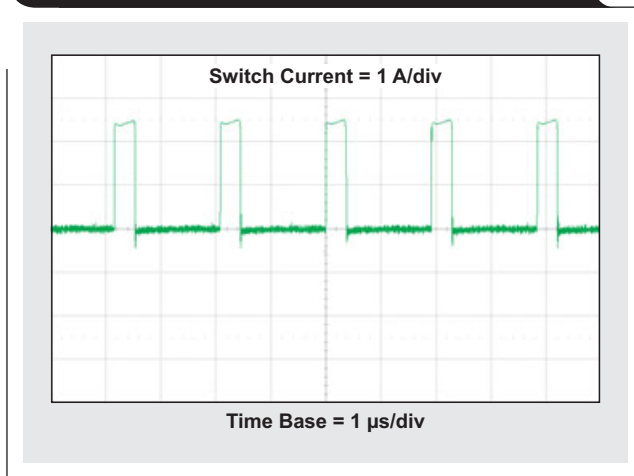
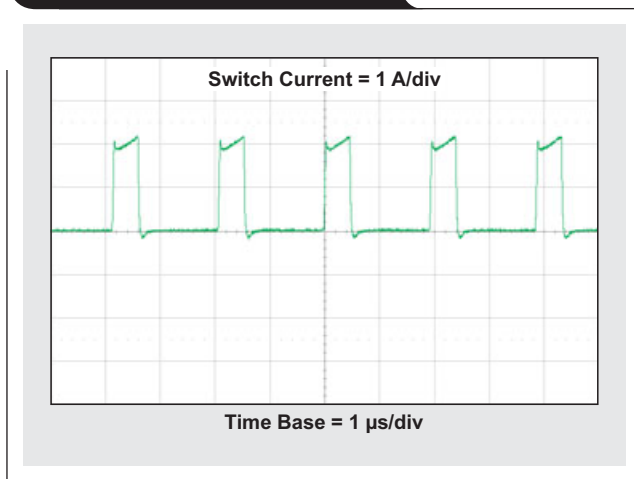


Figure 4. Buck output voltage ripple and switching-node voltage



Figure 6. Buck switch current



current, as the inductor is connected directly to the output. In this topology the output current is supplied by the inductor during both the on and off times. For the inverting buck-boost converter, this is not the case; so the average switch current during the on time is $I_{OUT}/(1 - D)$.

Input-voltage limitations

In addition to the converter's input-voltage constraint of $V_{IN} - (-V_{OUT})$, there may also be a limit to the input voltage at the low end besides that required by any minimum duty cycle or on-time specifications. Many DC/DC converter circuits include an undervoltage lockout (UVLO) circuit. In the buck configuration, the minimum input voltage would be limited by the UVLO level. This limitation exists for the inverting buck-boost converter as well; however, the UVLO threshold is relative to the device ground, which is configured as V_{OUT} . At start-up, the output is 0 V; so the minimum input voltage to guarantee proper start-up is equal to the UVLO level, regardless of the difference between V_{IN} and V_{OUT} .

Conclusion

A buck converter can be used to generate a negative output voltage from a positive input voltage if the circuit is configured as an inverting buck-boost converter. The circuit design is straightforward, but these important points should be remembered. The output current is less than

the average inductor current by a factor of $1 - D$, so the available output current will be less than the device rating. The output voltage is negative and is available at the device ground pin, so the effective voltage across the input of the device is $V_{IN} - V_{OUT}$. This difference must not exceed the input-voltage rating of the device. Finally, the ground of the device should not be tied to the system ground.

For a detailed design example using this technique, see Reference 2.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace "litnumber" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "The Right-Half-Plane Zero—A Simplified Explanation"slup084
2. John Tucker, "Using the TPS5430 as an Inverting Buck-Boost Converter," Application Reportslva257

Related Web sites

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